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A Novel Vernier-based Time to Digital Converter for Low-power RFID Sensor Tags

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Abstract

Power consumption is a key factor in analogue and digital design for portable devices. Radio Frequency Identification (RFID) is widely used in industry, military and medical purposes. This technology operates with very low power consumption. Power consumption in passive tags is negligible and in fact, power consumption delimits the sensor tag's life-time and range.

Many methods are proposed to reduce the RFID's power consumption, but new researches are demanded due to technological advancements and application growth. In this research, a new scheme for time-to-digital converter was proposed which consumes a significant amount of energy in sensor tags. This method preserves accuracy and speed in measurement while reducing the area used by the circuit as well as power consumption by a significant amount.

Keywords: *RFID, Low Power Design, Tag, Time-To-Digital Converter, Verinier, Sensor, TDC.*

1. Introduction

Radio frequency identification (RFID) mostly indicates systems which transmit a subject's ID number using a wireless technology. Barcode Technology was widely used before RFID for a touchless recognition, but now barcode readers cannot provide basic advantages of RFID. Although they are inexpensive, but they have some weaknesses, e.g., low capacity and unprogrammability.

Recently, combinations of RFID with different smart tags are pervasively used. This combination led to the creation of a new category of wireless sensor tags which emphasizes RFID's importance and provides new applications [1]. Sensor tags traditional structure is based on generating a sensitive voltage or current which is sensitive to a physical magnitude and eventually converting it to a digital code by an analogue to digital converter. On the other hand, analogue current or voltage processing circuits face more challenges as physical dimensions shrink. For example, reducing the voltage supply level makes the converter more sensitive to noise or increasing the threshold voltage causes other challenges [2-3], [18].

In sensor tags, it occurs when the power supply is produced by voltage multiplier but the utilizable current dramatically reduces by distance. A fundamental scheme was proposed to change the algorithms from physical magnitude-based to time delay-based to overcome traditional restrictions in ADC-based sensors [4]. Afterwards, another scheme based on time-to-digital converter (TDC) was proposed [5]. Therefore, a time interval sensitive to a physical magnitude was created. This interval was converted to a digital code by a TDC. Different methods were proposed to generate a time interval sensitive to different physical quantities [6], [7]. TDCs have high accuracy and operate with low voltage, low power and low area consumption. Therefore, converting a physical magnitude to time using TDC is a good idea for RFID sensor tags. Basically, there are three methods to measure the time interval between two asynchronous signals: analogue, digital and interpolation.

The analogue method is usually based on the measurement of the changes of a capacitor voltage which is charged by an invariable current during a charging time interval. The analogue method is very accurate and unique but its weaknesses are low stability (high noise-sensitivity) and non-linearity [8]. Thus, it is only usable for short time intervals measurement.

The interpolation method in signal processing is based on digital filtering techniques. This method has acceptable accuracy and is more stable compared to the analogue method. Although it has some weaknesses like artificial

estimations and complicated calculations and it needs a significant time interval for appropriate functioning.

The digital method is based on the number of a reference oscillator's clock cycles. This method is linear on a long time interval and its power consumption is acceptable. Its structure is more appropriate to be implemented in integrated circuits. It is more reliable in terms of noise sensitivity compared to analogue methods, but still its accuracy is restricted to the oscillator's period. To increase the accuracy, the oscillator's frequency must be increased which increases power consumption, while the power consumption is a vital parameter in RFID tags [8].

In order to increase the accuracy and reduce power consumption, several researches have been carried out on TDCs in RFID [8], [9-15].

A simple digital TDC is formed by an oscillator and a counter. A Start signal initiates the oscillator and finally a Stop signal pauses it. The counter counts the number of oscillations and eventually time intervals between the Start and Stop can be found by the number of counter multiplied by oscillator period. In Fig.1 counting the number of oscillator periods by a digital TDC is shown.

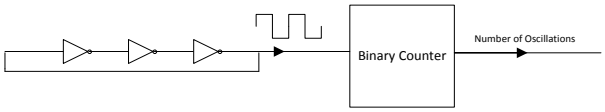

Fig. 1 The number of oscillations

This structure is simple but not accurate. As it is shown, the time inaccuracy is possible up to one oscillator period which is not acceptable in sensitive sensory tags.

The most important challenge of TDC design in RFID passive tags is to minimize the power consumption. A Sensor tag's general structure which uses a TDC to measure the time intervals is shown in Fig.2 [1], [2].

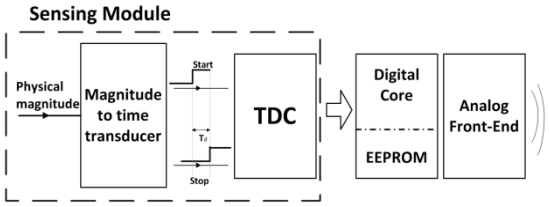

Fig. 2 Sensor tag's general structure

The analogue front-end, digital section and EEPROM are elements which are used in typical sensor tags. Sensing module is an extended block which is designed for RFID sensor tags. This block includes a magnitude to time converter section and TDC. The magnitude to time converter generates two signals which are Start and Stop. The duration between the start and stop rising edges (T_d) is a measurable magnitude. The Start and Stop signals are processed by TDC to generate a digital code. This code can be passed to the digital section and a sensed (measured) magnitude is sent to the reader. In the following section, the latest version of TDC will be introduced and compared with the other researches.

2. Vernier-based Time-to-digital Converter

Fig.2 shows the general structure of Vernier-based TDC designed for RFID sensor tag. This method is also known as Nonius design [16, 2].

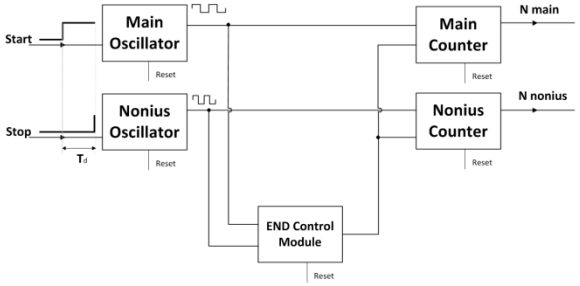

Fig. 3 Nonius TDC structure

According to [17], measurement accuracy can be optimized using two oscillators and two counters.

In this section, new ideas of measuring the time interval with the aim of reducing the power consumption will be introduced. In fact, the proposed method is based on Vernier method. As shown above, in Vernier method, there are two oscillators, which the first one starts with the Start signal and the other starts with the Stop signal. Fig.4 shows the time diagram for both oscillators. Signals 1 and 2 are the output signals for oscillators 1 and 2, respectively.

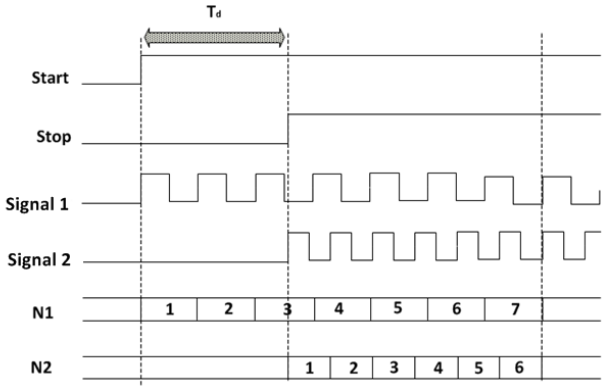

Fig. 4 Time graph in Vernier method

Two oscillators and two counters are utilized in order to increase measurement accuracy. As it is shown in above, the time lapse between the Start and Stop signals is two to three times multiplied by Oscillator 1 period. But in order to recognize the non-integer value of counter N1, another oscillator with shorter period than oscillator 1 must be used. In this case, the non-integer value of counter N1is reachable as well. When two oscillators are synchronized, it means both counters are showing integer values. The time interval between the Start and Stop signal can be estimated by:

$$T_d = N_1 T_1 - N_2 T_2 \quad (1)$$

Where T1 and T2 are signal 1 and 2 periods, respectively and T_d is exactly the time between Start and Stop which must be measured. Thus, in this case in order to measure this time interval, two oscillators and two counters are required.

3. The Proposed Design

3.1 Signal Synchronization

Assume that we divide the time required for measurement (Td) into two sections. As shown in Fig.5, section ΔT1 which equals to the section dividable by T1 and section δ1 which is the remainder of Td time. In fact, calculating this remainder section is of paramount importance, for if this section is ignored, there might be an error up to one period of signal 1 which is unacceptable for accurate sensing functions in RFID sensor tags.

$$N_2 \times T_1 - N_1 \times T_1 = K \times T_1$$

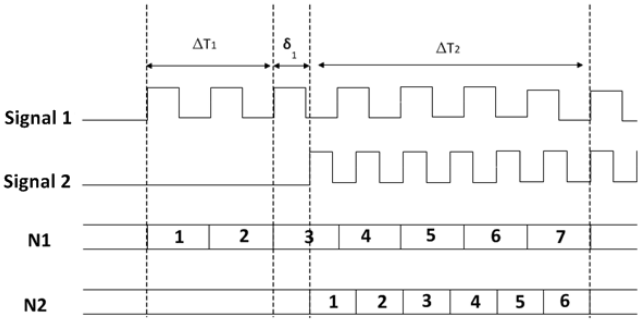

Fig. 5 Time graph in Vernier method

The remainder of time which is shown by ΔT2 is equal to the section dividable by T2. Thus, Td can be calculated using the following formula:

$$T_d = \Delta T_1 + \delta 1 \quad (2)$$

ΔT_2 equals the time in which two oscillators are synchronized. That means ΔT2 is the time interval required for signal 2 to pass signal 1. In fact, this time interval is the required time to compensate for δ1 time interval.

Now, assume the state in which two signals are synchronized at the beginning and the end of ΔT time interval, according to Fig. 6, the periods of signals 1 and 2 or T_1 and T_2 follow the following equations.

$$T_1 = \Delta T / N_1$$
$$T_2 = \Delta T / N_2 \quad (3)$$

That means T_1/T_2 ratio equals N_2/N_1.

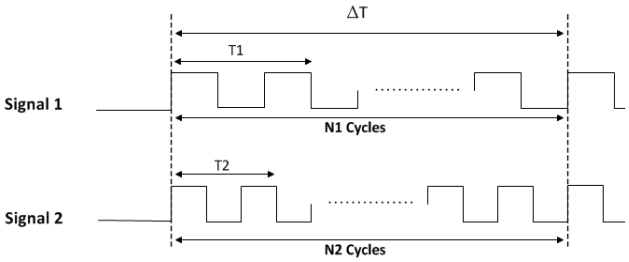

Fig. 6 two signals synchronized at the beginning and the end of the time interval

Assuming $T_1 > T_2$, it can be concluded that :

$$N_2 = N_1 + K \quad , (K \in Z > 0)$$
$$N_2 - N_1 = K \quad (4)$$

This means signal 1 oscillated k times less than signal 2.

Multiplying signal 1 period by the equation's both sides will yield:

Because $N_1 \times T_1 = N_2 \times T_2$:

$$N_2 \times T_1 - N_2 \times T_2 = K \times T_1 \rightarrow$$
$$\frac{N_2 \times T_1 - N_2 \times T_2}{T_1} = K$$
$$\rightarrow$$
$$\frac{N_2 \times (T_1 - T_2)}{T_1} = K \quad (5)$$

The above function means if T1/T2 ratio is determined, in order to recognize the oscillation difference between the

two signals in this interval (k), only one cycle i.e., N2 is needed. Thus, in order to recognize **K,** both cycles counts (N1, N2) are not necessary.

3.2 Signals' Conditions in Time-to-digital Converter

In TDC, the conditions are different. As shown in Fig.7, the outputs of the two oscillators are not synchronized at the start of oscillator 2 which is concurrent to the Stop signal's edge. In fact, this phase difference makes the number of cycles in signal 1non-integer. This is the value for measuring which the TDC is expanded and improved.

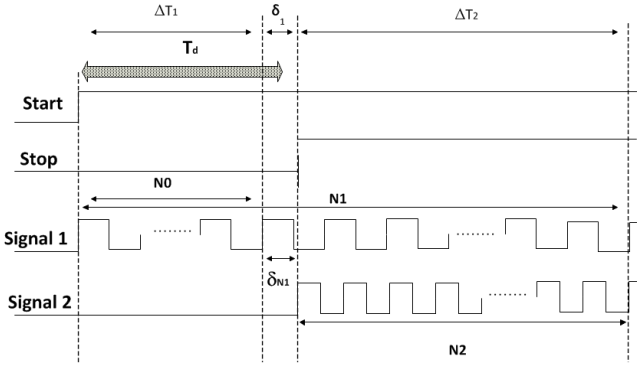

Fig. 7 non-integer portion of the last period of signal 1.

In ΔT2 interval, signal 2 oscillated exactly N2 times. According to two signals' periods ratio (T1/T2), the number of oscillations of signal 1 in this interval equals:

$$\frac{T_2}{T_1} \times N_2$$

Which is undoubtedly non-integer[1] and smaller than N2. That means difference between N_2 factor and 1, is the N2 factor in the non-integer portion before the Stop signal, that is:

$$1 - \frac{T_2}{T_1} \qquad (6)$$

As it is shown in Fig.7, N2 is the number of oscillations which synchronizes the two signals. It means N2 is the compensator of non-integer portion of signal 1 in time interval ΔT2.

The non-integer fraction before the time interval (ΔT2) is given by:

$$\delta_{N1} = \frac{T_1 - T_2}{T_1} \times N_2 \qquad (7)$$

[1]- In some T1/T2 ratios, signals 1 and 2 can never be synchronized.

Thus the number of oscillations of signal 1 in ΔT1 + δ1 time interval equals: $N_0 + \delta N1$

In which N0 is the integer number of signal 1 oscillations in the interval. Then, given this number multiplied by signal 1 period, the time in question can be calculated as:

$$T_d = (N_0 + \delta_{N1}) \times T_1 \qquad (8)$$

The above equation means in order to measure the time between Start and Stop, we only need the number of oscillations of one signal. Thus, during the whole measuring time measurement of only one magnitude is necessary which leads to the omission of one counter in Vernier method. Thus, the system can be redesigned so that it contains only one counter.

3.3 The Circuit Design

The proposed TDC is shown schematically in Fig.8.

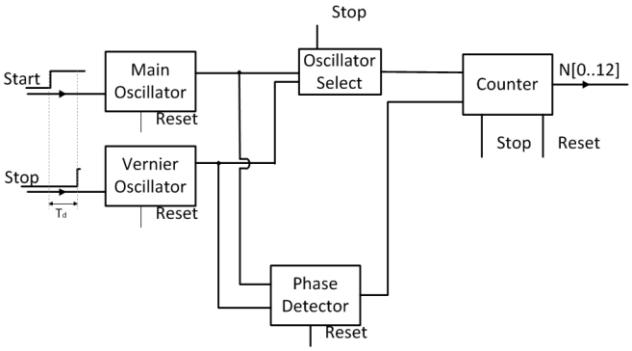

Fig. 8 Proposed system structure

The circuit includes two oscillators, Main and Vernier. These two oscillators are of digital ring oscillator type. The NAND gates delay causes the oscillation in output loop. Each oscillator's frequency is a function of all gates delay and the number of the gates must be determined, considering the production technology. Fig.9 shows a NAND based ring oscillator structure.

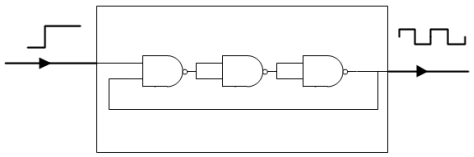

Fig. 9 NAND based ring oscillator

Both oscillators outputs are passed to Oscillator Select module and one of them passes to the counter based on demand. In Fig. 10, an Oscillator Select module is shown. As the Stop signal is activated, the module's output switches from Main to Vernier.

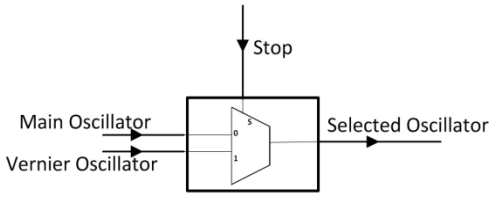

Fig. 10 Oscillator Select module

A Phase Detector module is also used to determine the Main and Vernier synchronization moment. This moment is the end of measurement period. The Phase Detector module's structure is shown in Fig.11.

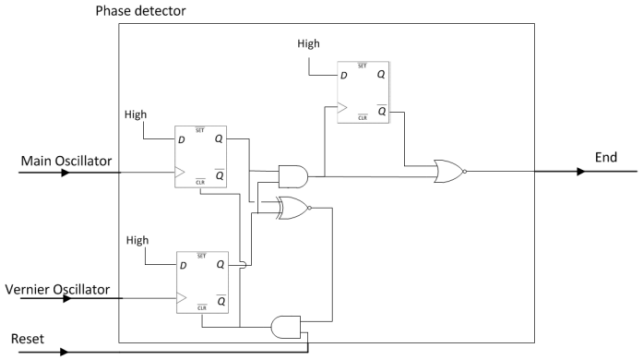

Fig. 11 Phase Detector Module Structure

The counter section counts the number of edges in its input signal.

3.4 Timing

As the Start signal is activated, the Main oscillator begins to act and its output is passed to the counter. When the Stop signal is activated, several tasks are done:

1. The counter's content is stored in the next level's latch which is the Digital Core.
2. Vernier oscillator begins functioning.
3. The counter is reset.
4. The oscillator select module switches and passes the Vernier oscillator's output to the counter.

Figure 12 shows the time diagram for TDC circuit. As it is shown, the counter counts the number of the Main oscillator's oscillations before the Stop signal and when the Stop signal is activated, it resets and begins counting the Vernier oscillator's oscillations. The END signal is the Phase Detector's output and indicates the end of the measuring process. As the END signal is activated, the counter stops and its content is stored in the Digital Core latch and both oscillators stop working.

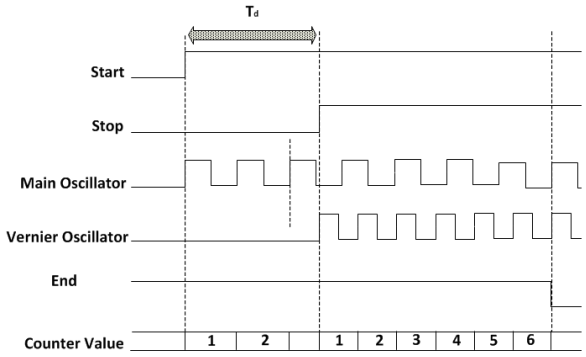

Fig. 12 Time graph for the proposed system

Using this method, at the end of each measuring cycle, two numbers will be latched in the output one of which is the integer number of the Main oscillator's oscillations before the Stop signal and the other one is the number of Vernier oscillator's oscillations before the synchronization of its output signal with the Main oscillator. Using the 8-3 function, the time between the Start and Stop signals can be calculated.

The following diagram shows the output waveform for the circuit designed by VHDL code in which the designed circuit's functionality is shown.

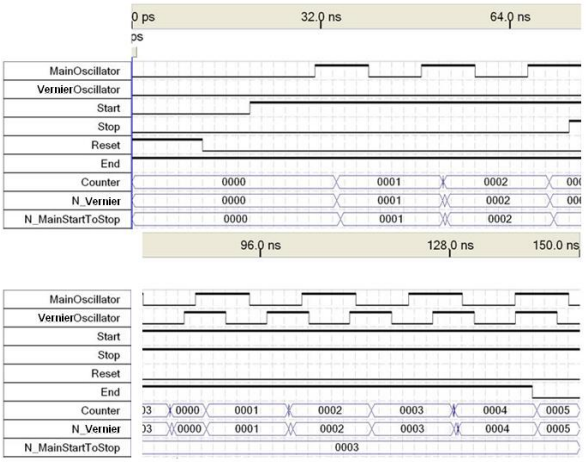

Fig. 13 VHDL code waveform of the proposed circuit.

We designed the TDC circuit in a way that it only needs one counter. Omission of one counter reduces the area and power consumption in Nonius design [17] and we will investigate the new scheme's circuit characteristics and compare them with the traditional designs.

4. Simulation

We utilized the Cadence software to simulate the circuit, and MOSFET 0.18um is the technology used in this simulation. Circuit's output waveform in 130ns Simulation is shown in Fig.14 to Fig.16. The simulation working frequency and input time interval are respectively assumed as 1 GHz and 10 ns.

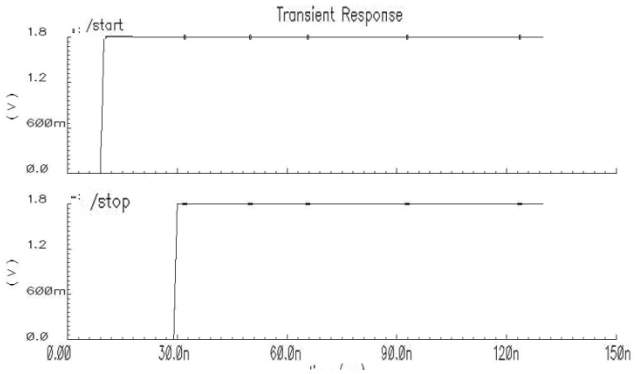

Fig. 14 Stop, Start waveform

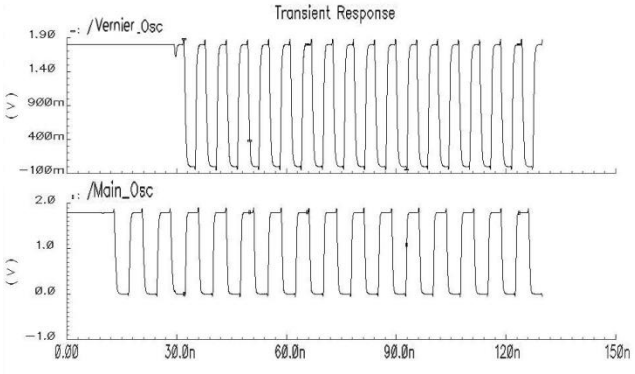

Fig. 15 Vernier and Main Oscillators Output.

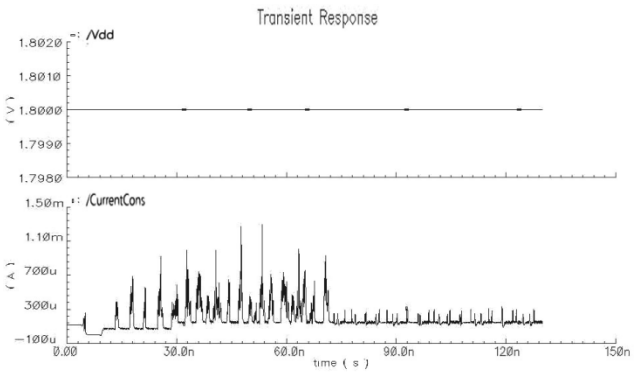

Fig. 16 Current Consumption and voltage supply waveform.

4.1 Power Consumption

In table 1, the power consumption of the proposed method is compared to that of the traditional schemes which indicates about 14% reduction compared to Nonius design.

Table 1: Comparison with previously reported TDCs

Structure	***Conversion time***	***Power consumption (uW)***
RSA TDC[17]	180 ns	900
Nonius TDC	130 ns	420
This work	130 ns	362

4.2 Layout and Area Consumption

The layout design for the proposed circuit is shown in Fig.17.

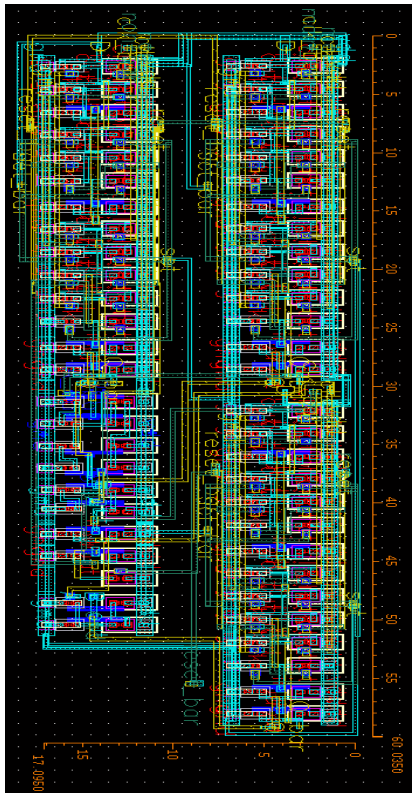

Fig. 17 Layout design for the proposed circuit

In table 2, the area consumption of the proposed method is compared to Nonius TDC. As it is manifest in the Table, the area consumption reduced about 25% in our method.

Table 2: Area consumption in the proposed method compared to Vernier method

Structure	***Area consumption***
Nonius TDC	80 um x 17 um
This work	60 um x 17 um

5. Conclusion

RFID sensor tags are pervasively used. Thus, in this research, it was tried to investigate their performance improvement. The most important factor influencing performance is power consumption. The power consumption for typical RFID tags is about microwatts which show how important design improvement is in their circuits. In this paper, an improved design for time-to-digital converter was proposed. According to the simulation results, power consumption and area consumption overtakes all traditional designs. In conclusion, this method can replace prevalent designs in RFID sensor tags.

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